



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/693,986	10/28/2003	Hyun-Ho Park	1572.1189	3975
21171 7590 07/31/2007 STAAS & HALSEY LLP SUITE 700 1201 NEW YORK AVENUE, N.W. WASHINGTON, DC 20005			EXAMINER LAMARRE, GUY J	
			ART UNIT 2112	PAPER NUMBER
			MAIL DATE 07/31/2007	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/693,986	Applicant(s) PARK ET AL.	
	Examiner Guy J. Lamarre	Art Unit 2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 07 May 2007 and 03 January 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) 24 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-23 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 October 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Amendment

0.1 **Claim 24** is withdrawn from consideration as being directed to a non-elected group.

Claims 1-23 remain pending.

0.2 The prior art rejections of record to **Claims 1-24** are withdrawn in response to Applicants' amendment of 5/7/2007 and 1/3/2007.

Response to Arguments

* Applicants' arguments, filed 1/3/2007, have been fully considered and are deemed persuasive only to the extent that the approach, whereby 'virtual data block,' is not specifically disclosed by the prior art of record. USPN 5933592 to **Lubbers et al.** discloses such procedures for virtual data block allocation as claimed.

Claim Rejections - 35 USC ' 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2.0 This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

2.1 **Claims 1-23** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Amelia** (US Patent No. 6,351,838) and **Lubbers et al.** (US Patent No. 5933592)

As per Claims 1, 13, 19, 22-23, Amelia substantially discloses, in Fig. 2 and related description, equivalent multidimensional storage system comprising multiple disk drives along with plural dimensional error detection/correction/protection along with appropriate controller capability, e.g., Amelia's 'FIG. 2 shows symmetrical three-dimensional parity protection system schematically as diagram 51 embodied by frame 53, with three two-dimensional planes 55, 57 and 59 with each plane containing conventional data storage disk drives such as disk drive 61 and parity protection disk drives for secondary storage data such as drive 63. In this simplified embodiment, each of the flat plane arrays 55, 57 and 59 are similar to the two-dimensional system shown in FIG. 1, and are connected similarly within each plane, but additionally, each flat plane has all of the drives connected to the other planes in a Z axis manner to create a three-dimensional parity protection system such as described above.'

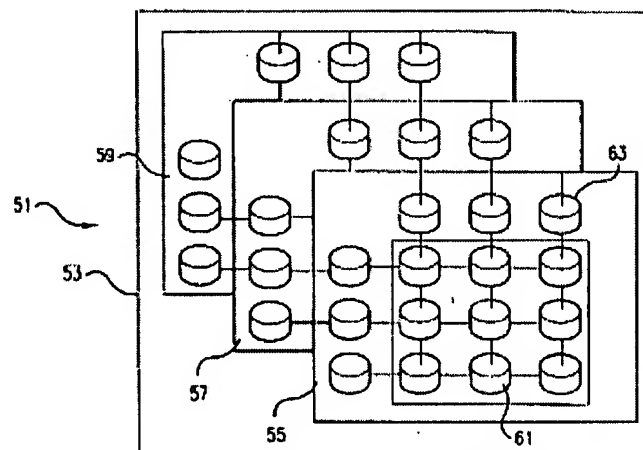


FIG. 2

Not specifically described in detail in Amelia is the step whereby data allocation comprises allocating data as virtual data along with corresponding virtual blocks.

However Lubbers et al., in an analogous art, discloses a "Promoting device level error to raidset level error to restore redundancy in a raid array data storage system," wherein such

techniques are described. {See **Lubbers et al.**, Id., Figs. -12, e.g., “The RAIDset metadata provides information about the RAIDed or RAID protected user data blocks in the entire virtual set of user data blocks. It is not limited to each drive as was the device metadata described immediately above. Virtual set refers to the user data blocks (but not the parity blocks) distributed across the drives A-D in the RAID array. In other words, in the example in FIG. 1, the virtual set consists of user data blocks O-N. To a host CPU using the RAID array a virtual set looks like a virtual disk drive having O-N data blocks.}

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the procedure in **Amelia** by including therein virtual set of user data block means as taught by **Lubbers et al.**, because such modification would provide the procedure disclosed in **Amelia** with a technique whereby “The RAIDset metadata provides information about the RAIDed or RAID protected user data blocks in the entire virtual set of user data blocks. It is not limited to each drive as was the device metadata described immediately above.” in **Lubbers et al.**}

As per Claim 2, Amelia discloses, in Fig. 2 and related description, equivalent multidimensional parity storing method according to claim 1, wherein the number of the storage blocks to be used as data blocks and the number of the storage blocks to be used as parity blocks are determined by calculating a maximum integer M satisfying $K \geq M^3 + 3M$, where K is the total number of storage blocks of the disk drives, so that the number of the data blocks is defined as M^3 and the number of the parity blocks is defined as $3M$ and the three-dimensional block matrix is a type of $M \times M \times M$. **As per Claim 3, Amelia discloses, in Fig. 2 and related description, equivalent multidimensional** parity storing method according to claim 1, wherein the allocating of the virtual data blocks and the virtual parity blocks to the storage blocks of the disk drives is

Art Unit: 2112

performed by allocating the virtual parity block for each block plane to the storage block of the disk drive after the virtual data blocks belonging to each block plane are completely allocated to the storage blocks of the disk drives.

As per Claim 4, Amelia discloses, in Fig. 2 and related description, equivalent multidimensional parity storing method according to claim 1, wherein the calculating of the parity information is performed by a bitwise operator performing exclusive OR (XOR) operation between the data bits stored in the storage blocks corresponding to the virtual data blocks of each block plane.

As per Claim 5, Amelia discloses, in Fig. 2 and related description, equivalent multidimensional error block recovery method in an external storage subsystem comprising multiple disk drives including a plurality of storage blocks, comprising: storing data and parity information by the parity storing method according to claim 1; and recovering a plurality of error blocks by using parity blocks corresponding to the virtual parity blocks related to the respective block planes with the error blocks of X, Y and Z-coordinates.

As per Claim 6, Amelia discloses, in Fig. 2 and related description, equivalent multidimensional n error block recovering method in an external storage subsystem comprising multiple disk drives including a plurality of storage blocks, comprising: storing data and parity information by the parity storing method according to claim 2; and recovering a plurality of error blocks by using the parity blocks corresponding to the virtual parity blocks related to the respective block planes with the error blocks of X, Y and Z-coordinates.

As per Claim 7, Amelia discloses, in Fig. 2 and related description, equivalent multidimensional n error block recovering method in an external storage subsystem comprising multiple disk drives including a plurality of storage blocks, comprising: storing data and parity information by the parity storing method according to claim 3; and recovering a plurality of error

Art Unit: 2112

blocks by using the parity blocks corresponding to the virtual parity blocks related to the respective block planes with the error blocks of X, Y and Z-coordinates.

As per Claim 8, Amelia discloses, in Fig. 2 and related description, equivalent multidimensional n error block recovering method in an external storage subsystem comprising multiple disk drives including a plurality of storage blocks, comprising: storing data and parity information by the parity storing method according to claim 4; and recovering a plurality of error blocks by using the parity blocks corresponding to the virtual parity blocks related to the respective block planes with the error blocks of X, Y and Z-coordinates.

As per Claim 9, Amelia discloses, in Fig. 2 and related description, equivalent multidimensional error block recovering method according to claim 5, wherein the recovering the plurality of error blocks comprises: counting the total numbers of the error blocks occurring in the block planes, respectively; skipping the block planes with no error blocks or with two or more error blocks performing an exclusive OR (XOR) operation between the data bits stored in the storage blocks, except for an error block, corresponding to the virtual data blocks belonging to each block plane with one error block; recovering the one error block by comparing XOR operation results with the parity information stored in the storage block corresponding to the parity block for the block plane; and repeating the above recovering operations in regular order of the X, Y and Z-coordinates.

As per Claim 10, Amelia discloses, in Fig. 2 and related description, equivalent multidimensional error block recovering method according to claim 6, wherein the recovering the plurality of error blocks comprises: counting the total numbers of the error blocks occurring in the block planes, respectively; skipping the block planes with no error blocks or with two or more error blocks each block plane with one error block; recovering the one error block by comparing XOR operation results with the parity information stored in the storage block

Art Unit: 2112

corresponding to the parity block for the block plane; and repeating the above recovering operations in regular order of the X, Y and Z-coordinates.

As per Claim 11, Amelia discloses, in Fig. 2 and related description, equivalent multidimensional error block recovering method according to claim 7, wherein the recovering the plurality of error blocks comprises: counting the total numbers of the error blocks occurring in the block planes, respectively; skipping the block planes with no error blocks or with two or more error blocks performing an exclusive OR (XOR) operation between the data bits stored in the storage blocks, except for an error block, corresponding to the virtual data blocks belonging to the block plane with one error block; recovering the one error block by comparing XOR operation results with the parity information stored in the storage block corresponding to the parity block for the block plane; and repeating the above recovering operations in regular order of the X, Y and Z-coordinates.

As per Claim 12, Amelia discloses, in Fig. 2 and related description, equivalent multidimensional error block recovering method according to claim 8, wherein the recovering the plurality of error blocks comprises: counting the total numbers of the error blocks occurring in the block planes, respectively; skipping the block planes with no error blocks or with two or more error blocks performing an exclusive OR (XOR) operation between the data bits stored in the storage blocks, except for an error block, corresponding to the virtual data blocks belonging to the block plane with one error block; recovering the one error block by comparing XOR operation results with the parity information stored in the storage block corresponding to the parity block for the block plane; and repeating the above recovering operations in regular order of the X, Y and Z-coordinates.

As per Claim 14, Amelia discloses, in Fig. 2 and related description, equivalent multidimensional storage of claim 13, wherein the programmed computer processor further

calculates parity information based upon the data bits respectively stored in the storage blocks corresponding to the virtual data blocks of each virtual data block plane.

As per Claim 15, Amelia discloses, in Fig. 2 and related description, equivalent multidimensional storage of claim 13, wherein the programmed computer processor further recovers any number of error blocks in the storage blocks according to the virtual parity blocks corresponding to each virtual data block plane.

As per Claim 16, Amelia discloses, in Fig. 2 and related description, equivalent multidimensional storage of claim 13, wherein the programmed computer processor generates the virtual three-dimensional block matrix by calculating a maximum integer M satisfying $K \geq M^3 + 3M$, where K is the total number of storage blocks of the disk drives, M^3 is a number of the storage blocks used as data blocks, and $3M$ is a number of the storage blocks used as parity blocks, and the three-dimensional block matrix is $M \times M \times M$.

As per Claim 17, Amelia discloses, in Fig. 2 and related description, equivalent multidimensional storage of claim 15, wherein the programmed computer processor recovers the error blocks by repetitively: counting a total number of the error blocks occurring in the virtual data block planes, respectively, skipping the virtual data block planes with no error blocks or with two or more error blocks, performing an exclusive OR (XOR) operation between the data bits stored in the storage blocks, except for an error block, corresponding to the virtual data blocks belonging to the virtual data block plane with one error block, and recovering the one error block by comparing the XOR operation results with the parity information stored in the storage block corresponding to the virtual parity block for the virtual data block plane.

As per Claim 18, Amelia discloses, in Fig. 2 and related description, equivalent multidimensional storage of claim 13, wherein the programmed computer processor associates the storage blocks of the disk drives to the virtual three-dimensional block matrix by:

determining a number of the storage blocks to be used as data blocks and a number of the storage blocks to be used as parity blocks in a total number of storage blocks of the disk drives, generating the three-dimensional block matrix of the virtual data blocks corresponding to the determined number of the storage blocks to be used as the data blocks on Cartesian coordinates (X, Y, Z), allocating the virtual parity blocks to the virtual data block planes related to the X, Y and Z-coordinates of the three-dimensional block matrix, respectively, allocating the virtual data blocks and the virtual parity blocks to the storage blocks of the disk drives, respectively, calculating parity information based upon the data bits respectively stored in the storage blocks corresponding to the virtual data blocks of every virtual data block plane, and storing the calculated parity information in the storage blocks corresponding to the virtual parity blocks for every virtual data block plane, respectively.

As per Claim 20, Amelia discloses, in Fig. 2 and related description, equivalent multidimensional system of claim 19, wherein the controller further calculates parity information based upon the data bits respectively stored in the storage blocks corresponding to the virtual data blocks of each virtual block plane.

As per Claim 21, Amelia discloses, in Fig. 2 and related description, equivalent multidimensional system of claim 19, wherein the controller further recovers any number of error blocks in the storage blocks according to the virtual parity blocks corresponding to each virtual data block plane.

CONCLUSION

* Any response to this action should be mailed to:

Commissioner of Patents and Trademarks, Washington, D.C. 20231

or faxed to: (571) 273-8300 for all formal communications.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Guy J. Lamarre, P.E., whose telephone number is (571) 272-3826. The examiner can normally be reached on Monday to Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques, can be reached at (571) 272-6962.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-3609.

Information regarding the status of an application may also be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Guy J. Lamarre, P.E.
Primary Examiner
7/23/2007
